3. Hardware

3.1 Computer architecture

1 (a) One of the key features of von Neumann computer architecture is the use of buses.

Three buses and three descriptions are shown below.

Draw a line to connect each bus to its correct description.

Bus	Description
address bus	this bus carries signals used to coordinate the computer's activities
control bus	this bi-directional bus is used to exchange data between processor, memory and input/ output devices
data bus	this uni-directional bus carries signals relating to memory addresses between processor and memory

(b) The seven stages in a von Neumann fetch-execute cycle are shown in the table below.

Put each stage in the correct sequence by writing the numbers 1 to 7 in the right hand column. The first one has been done for you.

Stage	Sequence number
the instruction is then copied from the memory location contained in the MAR (memory address register) and is placed in the MDR (memory data register)	
the instruction is finally decoded and is then executed	
the PC (program counter) contains the address of the next instruction to be fetched	**1**
the entire instruction is then copied from the MDR (memory data register) and placed in the CIR (current instruction register)	
the address contained in the PC (program counter) is copied to the MAR (memory address register) via the address bus	
the address part of the instruction, if any, is placed in the MAR (memory address register)	
the value in the PC (program counter) is then incremented so that it points to the next instruction to be fetched	

[6]

2 (b) Two features of Von Neumann architecture are the use of registers and the use of buses.

Give the names of **two** registers and **two** buses.

Registers

1 .....

.....

2 .....

.....

Buses

1 .....

.....

2 .....

.....

[4]

3 A section of computer memory is shown below:

Address	Contents
1000 0000	0110 1110
1000 0001	0101 0001
1000 0010	1000 1101
1000 0011	1000 1100
≀	≀
1000 1100	
1000 1101	
1000 1110	
1000 1111	

(a) (i) The contents of memory location 1000 0001 are to be read.

Show the contents of the Memory Address Register (MAR) and the Memory Data Register (MDR) during this read operation:

MAR | | | | | | | | |

MDR | | | | | | | | |

[2]

(ii) The value 0111 1001 is to be written into memory location 1000 1110.

Show the contents of the MAR and MDR during this write operation:

MAR | | | | | | | | |

MDR | | | | | | | | |

[2]

(iii) Show any changes to the computer memory following the read and write operations in **part (a)(i)** and **part (a)(ii)**.

Address	Contents
1000 0000	0110 1110
1000 0001	0101 0001
1000 0010	1000 1101
1000 0011	1000 1100
1000 1100	
1000 1101	
1000 1110	
1000 1111	

[1]

(b) Name **three** other registers used in computers.

1 .....

2 .....

3 .....

[3]

(c) The control unit is part of a computer system.

What is the function of the control unit?

.....

.....

.....

.....

.....

..... [3]

4 To process an instruction, a central processing unit (CPU) goes through a cycle that has three main stages.

Name each stage in this cycle.

Stage 1 .....

Stage 2 .....

Stage 3 .....

[3]

5 **Four** computer terms and **eight** descriptions are shown below.

Draw lines to connect each computer term to the correct description(s).

Computer term	Description
Arithmetic and logic unit (ALU)	Carries out operations such as addition and multiplication
Control unit	Fetches each instruction in turn
Random access memory (RAM)	Stores data currently in use
Read only memory (ROM)	Stores bootstrap loader and BIOS
	Stores part of the operating system currently in use
	Carries out operations such as AND, OR, NOT
	Data can be read but not altered
	Manages execution of each instruction

[4]

6 Signals are sent to and from the components of a processor using buses.

Identify and describe the purpose of **two** different buses.

Bus 1 .....

Purpose .....

.....

.....

.....

.....

.....

Bus 2 .....

Purpose .....

.....

.....

.....

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.....

[6]

7 Name **three** different buses that are used in the fetch-execute cycle.

Bus 1 .....

Bus 2 .....

Bus 3 .....

[3]

8 **Six** components of a computer system and **six** descriptions are shown.

Draw a line to match each component with the most suitable description.

Component	Description
Arithmetic Logic Unit (ALU)	Used to connect together the internal components of the CPU.
Buses	Used to carry out calculations on data.
Control Unit (CU)	Used to temporarily hold data and instructions during processing.
Immediate Access Store (IAS)	Used to allow interaction with the computer.
Input/Output	Used to hold data and instructions before they are processed.
Registers	Used to manage the flow of data through the CPU.

[5]

9 **Six** components of the Von Neumann model for a computer system and **six** descriptions are given.

Draw a line to match each component to the most suitable description.

Component	Description
Immediate access store (IAS)	Holds data and instructions when they are loaded from main memory and are waiting to be processed.
Register	Holds data temporarily that is currently being used in a calculation.
Control unit (CU)	Holds data or instructions temporarily when they are being processed.
Accumulator (ACC)	Manages the flow of data and interaction between the components of the processor.
Arithmetic logic unit (ALU)	Carries out the calculations on data.
Bus	Pathway for transmitting data and instructions.

[5]

10 Kelvin correctly answers an examination question about the Von Neumann model.

Eight different terms have been removed from his answer.

Complete the sentences in Kelvin's answer, using the list given.

Not all items in the list need to be used.

- accumulator (ACC)
- address bus
- arithmetic logic unit (ALU)
- control unit (CU)
- data bus
- executed
- fetches
- immediate access store (IAS)
- memory address register (MAR)
- memory data register (MDR)
- program counter (PC)
- saved
- transmits

The central processing unit (CPU) .....

the data and instructions needed and stores them in the

..... to wait to be processed.

The ..... holds the address of the next

instruction. This address is sent to the ..... .

The data from this address is sent to the ..... .

The instruction can then be decoded and ..... .

Any calculations that are carried out on the data are done by the

..... . During calculations, the data is temporarily

held in a register called the ..... .

[8]

11 Explain how an instruction is fetched in a computer based on the Von Neumann model.

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..... [6]

12 The fetch-execute cycle make use of registers.

(a) Describe the role of the Program Counter (PC).

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.....

.....

.....[2]

(b) Describe the role of the Memory Data Register (MDR).

.....

.....

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.....[2]

13 Vanessa writes a paragraph as an answer to an examination question about the central processing unit (CPU).

Use the list given to complete Vanessa's answer by inserting the correct **six** missing terms. Not all terms will be used.

- Components
- Data
- Decoded
- Executed
- Fetched
- Instructions
- RAM
- ROM
- Secondary storage

The CPU processes ..... and ..... .

An instruction is ..... from .....

into the CPU where it is then ..... . Once this has taken place the

instruction is then ..... .

[6]

14 **(a)** A computer can have both a MAC address and an IP address.

Four statements are given about MAC addresses and IP addresses.

Tick (✓) to show whether each statement is **True** or **False**.

Statement	True (✓)	False (✓)
A MAC address is unique to a computer on a network		
Once an IP address has been set it cannot be changed		
A MAC address is made up of the computer's serial number and the IP address		
If a computer does not have an IP address it cannot communicate with another device using the Internet		

[4]

(b) A computer uses the Von Neumann model and the stored program concept.

(i) Explain what is meant by the stored program concept.

.....

.....

.....

..... [2]

(ii) The Von Neumann model has several components that are used in the fetch-execute cycle.

One component is the Arithmetic Logic Unit (ALU).

Describe the role of the ALU.

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.....

..... [4]

(c) The computer has an operating system.

(i) A signal causes the operating system to stop and assess what to do next.

Identify the name of this signal.

..... [1]

(ii) State **two** functions of an operating system.

1 .....

2 .....

[2]

15 Explain how an instruction is fetched in a Von Neumann model computer.

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..... [6]

16 The Von Neumann model for a computer system uses several components in the fetch-execute cycle. One component that is used is the Control Unit (CU).

Identify **four** other components that are used in the Von Neumann model for a computer system.

1 .....

2 .....

3 .....

4 .....

[4]

17 The Von Neumann model for a computer system has several components that are used in the fetch-execute cycle.

(a) One component is main memory.

(i) Describe what is meant by main memory and how it is used in the Von Neumann model for a computer system.

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..... [3]

(ii) State **two** other components in the Von Neumann model for a computer system.

1 .....

2 .....

[2]

18 **Six** components of a computer are given.

Some are part of the central processing unit (CPU) of the Von Neumann model for a computer system.

Tick (✓) to show if each component is a **CPU component** or is **Not a CPU component**.

Component	CPU component (✓)	Not a CPU component (✓)
Arithmetic logic unit (ALU)		
Hard disk drive (HDD)		
Memory address register (MAR)		
Random access memory (RAM)		
Solid state drive (SSD)		
Control unit (CU)		

[6]

19 A Von Neumann model for a computer system has a central processing unit (CPU) that makes use of registers.

(a) Identify **three** registers that may be used.

Register 1 .....

Register 2 .....

Register 3 .....

[3]

(b) The CPU is responsible for processing instructions.

One stage of processing instructions is the decode stage.

(i) Identify the **two other** stages of processing instructions.

Stage 1 .....

Stage 2 .....

[2]

(ii) Identify the component of the CPU that is responsible for decoding instructions.

..... [1]

20 A Von Neumann model for a computer system contains several integrated circuits (IC).

(a) Parallel data transmission is used in an IC.

(i) Describe how data is transmitted using parallel data transmission.

.....

.....

.....

..... [2]

(ii) Give **one** benefit of using parallel, rather than serial, data transmission.

.....

..... [1]

(b) The computer has a central processing unit (CPU).

(i) Identify the bus that carries signals around the CPU to control the components.

..... [1]

(ii) Identify the register built into the arithmetic logic unit (ALU).

..... [1]

(iii) Four statements about a Von Neumann model for a computer system are shown.

Tick (✓) to show if each statement is **True** or **False**.

Statement	**True (✓)**	**False (✓)**
Data and instructions are stored in the same memory unit		
The control unit manages operations within the CPU		
Data and instructions can be fetched into the CPU at the same time		
The control unit is responsible for decoding an instruction		

[4]

21 Paige has a computer that has a central processing unit (CPU) based on the Von Neumann model for a computer system.

(a) Identify the component within the CPU that controls the flow of data.

..... [1]

(b) Identify the component within the CPU where calculations are carried out.

..... [1]

(c) Identify the component within the CPU that stores the address of the next instruction to be processed.

..... [1]

(d) Identify the register within the CPU that holds an instruction that has been fetched from memory.

..... [1]

(e) Identify the register within the CPU that holds data that has been fetched from memory.

..... [1]

22 Several components are involved in processing an instruction in a Von Neumann model for a computer system.

Three of these components are the arithmetic logic unit (ALU), control unit (CU) and random access memory (RAM).

(a) Six statements are given about the components.

Tick (✓) to show if each statement applies to the ALU, CU or the RAM. Some statements may apply to more than one component.

Statement	ALU (✓)	CU (✓)	RAM (✓)
stores data and instructions before they enter the central processing unit (CPU)			
contains a register called the accumulator			
manages the transmission of data and instructions to the correct components			
contained within the CPU			
uses the data bus to send data into or out of the CPU			
carries out calculations on data			

[6]

(b) The accumulator is a register that is part of the Von Neumann model.

Give **two** other registers that are part of the Von Neumann model.

1 .....

2 .....

[2]

23 **Six** statements are given about the role of components in the Central Processing Unit (CPU).

(a) Tick (✓) to show whether each statement applies to the Memory Address Register (MAR), Memory Data Register (MDR) or Program Counter (PC).

Some statements may apply to more than one component.

Statement	MAR (✓)	MDR (✓)	PC (✓)
it is a register in the CPU			
it holds the address of the next instruction to be processed			
it holds the address of the data that is about to be fetched from memory			
it holds the data that has been fetched from memory			
it receives signals from the control unit			
it uses the address bus to send an address to another component			

[6]

(b) Identify the component in the CPU that carries out calculations.

..... [1]

24 In a Von Neumann model for a computer system, a Central Processing Unit (CPU) contains a number of different components.

The table contains the name of a component or a description of their role in the fetch-execute cycle.

Complete the table with the missing component names and descriptions.

Component name	Description
Memory Address Register (MAR)	....
Program Counter (PC)	....
.....	This is a register that is built into the arithmetic logic unit. It temporarily holds the result of a calculation.
.....	This is a register that holds data or an instruction that has been fetched from memory.
Control Unit (CU)	....
.....	This carries addresses around the CPU.

[6]

25 Secondary storage devices are used to store data in a computer.

(a) Circle **three** components that are secondary storage devices.

central processing unit (CPU) compact disk (CD)

hard disk drive (HDD) random access memory (RAM) read only memory (ROM)

register sensor solid-state drive (SSD)

[3]

(b) Tick (✓) **one** box to show which statement about secondary storage is correct.

A It is directly accessed by the CPU. ☐

B It is magnetic storage only. ☐

C It is used to permanently store software and data files. ☐

D It is volatile. ☐

[1]

26 A library has a self-checkout system that allows customers to register books that they want to borrow.

The self-checkout system has a central processing unit (CPU).

The CPU has two cores.

(a) State the purpose of a core in the CPU.

.....

..... [1]

(b) The CPU is replaced with one that has four cores.

Explain the effect this has on the performance of the self-checkout system.

.....

.....

.....

..... [2]

(c) The CPU contains registers and buses.

(i) Describe the role of a register in the CPU.

.....

.....

.....

..... [2]

(ii) Identify **one** bus that can be found in the CPU and explain its purpose in the fetch–decode–execute cycle.

Bus .....

Purpose .....

.....

.....

.....

[3]

27 **(c)** A component in the CPU sends signals to manage the fetch-decode-execute cycle.

State the name of this component.

..... [1]

(d) The CPU has a clock speed of 2.4 Ghz.

Describe what is meant by a 2.4 Ghz clock speed.

.....

.....

.....

..... [2]

(e) The CPU contains registers including the memory data register (MDR).

(i) Describe the role of the MDR in the fetch-decode-execute cycle.

.....

.....

.....

..... [2]

(ii) Identify **three** other registers contained in the CPU.

1 .....

2 .....

3 .....

[3]

28 A user's computer has a central processing unit (CPU) that has a clock speed of 2 GHz.

She wants to change it to a CPU that has a clock speed of 3 GHz.

(a) (i) State what is meant by clock speed.

.....

..... [1]

(ii) Explain the effect this change will have on the performance of the CPU.

.....

.....

.....

..... [2]

(b) The CPU contains a memory address register (MAR).

Describe the role of the MAR in the fetch–decode–execute cycle.

.....

.....

.....

..... [2]

(c) The CPU has a list of all the machine code commands it can process.

State the name of this list of commands.

..... [1]

29 A washing machine is an example of an embedded system.

(a) Give **two** characteristics of an embedded system.

1 .....

.....

2 .....

.....

[2]

(b) Circle **three** other examples of an embedded system.

freezer laptop

personal computer (PC) security light system smartphone

vending machine web server

[3]

30 A computer has a central processing unit (CPU).

(a) Circle **three** components that are built into the CPU.

accumulator (ACC) control unit (CU) graphics card

hard disk drive (HDD) motherboard program counter (PC)

random access memory (RAM) read only memory (ROM)

[3]

(b) The CPU has cache.

Explain the purpose of the cache.

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.....

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..... [2]

(c) The CPU has a component that regulates the number of fetch–decode–execute cycles the CPU can perform in a second.

State the name of this component.

..... [1]

(d) The CPU has a component that carries out all calculations and logical operations.

State the name of this component.

..... [1]

31 (d) The computer processes instructions using the fetch–decode–execute (FDE) cycle.

Draw and annotate a diagram to show the process of the **fetch** stage of the FDE cycle.

[4]

32 Instructions are processed by a central processing unit (CPU) in a computer.

(a) Complete the paragraph about fetching an instruction into the CPU to be processed.

Use the terms from the list.

Some of the terms in the list will **not** be used. You should only use a term once.

address arithmetic logic unit (ALU) binary control unit (CU)

current instruction register (CIR) data denary driver

fetch interrupt memory address register (MAR)

memory data register (MDR) random access memory (RAM)

read only memory (ROM) secondary storage signal

The program counter contains the ……

of the next instruction to be processed; this is then sent to the

…… using the address bus. The address is then

sent to the …… .

Once the address is received, the instruction stored at the location is

sent to the ……, using the

…… bus. The instruction is then

sent to the …… that is built into the

…… .

[7]

(b) The CPU uses an instruction set to decode the instruction.

State what is meant by an instruction set.

……

…… [1]

33 A student has a computer that has a central processing unit (CPU).

(a) Describe the role of the CPU in the computer.

.....

.....

.....

..... [2]

(b) The CPU contains registers.

(i) State the purpose of a register.

.....

..... [1]

(ii) Give **three** registers that are built into the CPU.

1 .....

2 .....

3 .....

[3]

(c) One component in the CPU is the arithmetic logic unit (ALU).

Describe the purpose of the ALU.

.....

.....

.....

.....

..... [3]

(d) The student wants to replace the CPU to increase the performance of the computer.

Explain why a different CPU can increase the performance.

.....

.....

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.....

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.....

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..... [4]

34 A central processing unit (CPU) performs the fetch–decode–execute (FDE) cycle.

(a) Give the name of **two** registers that are used in the fetch stage of the cycle.

1 .....

2 .....

[2]

(b) Describe what happens at the decode stage of the cycle.

.....

.....

.....

.....

.....

..... [3]

(c) Give **one** register in the CPU that is used in the execute stage of the cycle.

..... [1]

(d) Buses are used in the CPU to transmit data through the FDE cycle.

Circle **three** buses that are used in the CPU.

fetch	address	register	execute
data	decode	calculation	
central	value	binary	control

[3]

(e) A user changes their CPU from one with a dual core and a clock speed of 2.4 GHz to one with a dual core and a clock speed of 3.5 GHz.

Explain the effect this change will have on the performance of the CPU.

.....

.....

.....

..... [2]

35 The table contains names and descriptions of components in a central processing unit (CPU).

Complete the table by giving the missing component names and descriptions.

Component name	Description
.....	sends signals to manage the flow of data through the CPU
program counter	....
.....	stores the address of the data that is about to be fetched from random access memory (RAM) into the CPU
.....	transmits data between the RAM and the CPU
accumulator	....
.....	stores an instruction when it is being decoded

[6]

36 An instruction is fetched from random access memory (RAM) into the memory data register (MDR) to be decoded.

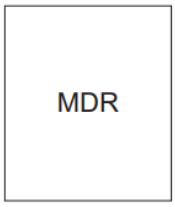
(a) Identify **two** other registers that are used in the fetch stage of the cycle.

1 .....

2 .....

[2]

(b) Complete and annotate the diagram to show how the data is decoded once it has been fetched into the MDR.



[4]